b. a circuit

for starting a phase locked loop when voltage applied by said first circuit exceeds a threshold, [and]

for inhibiting operation of at least a plurality of clocks until released, and

[c.] for releasing all inhibited clocks once voltage stability is achieved.

7. (Amended) The power on reset circuit of claim 1, wherein said power on reset circuit is contained within an integrated circuit.

REMARKS

I. STATUS OF THE APPLICATION

Claims 1-17 are pending in the application.

Claims 14-17 are withdrawn from consideration.

Claims 1-13 stand rejected under 35 U.S.C. §112, first paragraph.

Claims 1-13 stand rejected under 35 U.S.C. §112, second paragraph.

Claims 1, 6, 7, and 12 stand rejected under 35 U.S.C. §102(b).

Claims 1, 8, and 12 are the only independent claims under consideration.

II. AMENDMENTS

Claims 1 and 7 have been amended to place the claim in correct idiomatic English.

The specification has been amended to correct minor typographical errors. Applicants urge that no new matter has been added.

III. CLAIMS 1-13 ARE ENABLED WITHIN THE MEANING OF 35 U.S.C. § 112, FIRST PARAGRAPH

Claims 1-13 stand rejected under 35 U.S.C. § 112, first paragraph, as described in paragraph 5 of the Office Action.

Applicants respectfully traverse the rejection of claims 1-13 under 35 U.S.C. § 112, first paragraph for the following reasons.

In accordance with 35 U.S.C. § 112, first paragraph, even though the statute does not use the term "undue experimentation", it has been interpreted to require that the claimed invention be enabled so that any person skilled in the art can make and use the invention without undue experimentation. In re Wands, 858 F.2d at 737, 8 USPQ2d at 1404 (Fed. Cir. 1988). Applicants urge that the Examiner has failed to show that the claimed invention is not "enabled so that any person skilled in the art can make and use the invention without undue experimentation" in accordance with the eight factor test as outlined in MPEP § 2164.01(a).

Sufficient description for enablement of the power on reset circuit recited in independent claim 1 and the method of applying power recited in independent claims 8 and 12, may be found in the specification, for example, on page 30, line 23 through page 31, line 35. At least the circuitry described in this passage, and illustrated in Figure 23 and Figure 24, support claims 1, 8, and 12, and allows one of ordinary skill in the art to implement the claimed invention. The Applicants still further urge that one of skill in the art would understand the relationship between the PLL and the plurality of clocks upon reading the specification, for example, on page 30, line 23 through page 31, line 35, and illustrated in Figures 23-26.

Applicants respectfully submit that claims 1, 8, and 12 are enabled, and urge that the rejection of claims 1, 8, and 12, and the respective dependent claims, under 35 U.S.C. § 112, first paragraph be withdrawn.

IV. CLAIMS 1-13 ARE DEFINITE WITHIN THE MEANING OF 35 U.S.C. § 112, SECOND PARAGRAPH

Claims 1-13 stand rejected under 35 U.S.C. § 112, second paragraph, as described in paragraph 7 of the Office Action.

Applicants respectfully traverse the rejection of claims 1-13 under 35 U.S.C. § 112, second paragraph for the following reasons.

Clear and concise description of the power on reset circuit recited in independent claim 1 and the method of applying power recited in independent claims 8 and 12, may be found in the specification, for example, on page 30, line 23 through page 31, line 35. At least the circuitry described in this passage, and illustrated in Figure 23 and Figure 24, support claims 1, 8, and 12, and allows one of ordinary skill in the art to implement the claimed invention. The Applicants still further urge that one of skill in the art would understand the relationship between the PLL and the plurality of clocks upon reading the specification, for example, on page 30, line 23 through page 31, line 35, and illustrated in Figures 23-26.

Furthermore, since claims 2-7 are dependent upon claim 1, and therefore include all the limitations thereof, Applicants submit that claims 2-7 additionally are definite. Still further, claim 7 has been amended for grammatical correction.

Finally, since claims 9-11 and 13 are dependent upon claim 8, and therefore include all the limitations thereof, Applicants submit that claims 9-11 and 13 additionally are definite.

In view of the above remarks, Applicants respectfully submit that claims 1, 8, and 12 are definite, and urge that the rejection of claims 1, 8, and 12, and the respective dependent claims, under 35 U.S.C. § 112, second paragraph be withdrawn.

V. CLAIMS 1, 6, 7, AND 12 ARE NOVEL WITHIN THE MEANING OF 35 U.S.C. § 102(b) OVER SHAIK ET AL. BECAUSE THE APPLIED PRIOR ART FAILS TO TEACH STARTING A PLL AFTER A THESHOLD VOLTAGE IS EXCEEDED

Claims 1, 6, 7, and 12 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over Shaik et al. ("Shaik"), as described in paragraph 9 of the Office Action.

Applicants respectfully traverse the rejection of claims 1, 6, 7, and 12 under 35 U.S.C. § 102(b) for the following reasons.

Independent claim 1 recites *inter alia*, "a circuit for starting a phase locked loop when voltage applied by said first circuit exceeds a threshold."

Independent claim 12 recites *inter alia*, that " when a voltage applied to said integrated circuit exceeds a first threshold placing a hold on the operation of at least one clock on said integrated circuit and allowing a phase locked loop to start."

An example of starting a PLL after a first circuit exceeds a threshold may be found in the specification, for example, with respect to Figure 25 and the related text.

Shaik fails to teach at least the above identified features. On the contrary, Shaik merely teaches an ENABLE PLL signal, that may be set to 1 or 0. There is no discussion in the reference at to whether the ENABLE PLL signal is from the voltage applied to the

integrated circuit. More precisely, there is no discussion in the reference whether the ENABLE PLL signal is set to 1 when the voltage applied to the integrated circuit exceeds a threshold.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is clear that Shaik does not anticipate claims 1 or 12.

Furthermore, since claims 6 and 7 are dependent upon claim 1, and therefore include all the limitations thereof, Applicants submit that claims 6 and 7 additionally are not anticipated by Shaik.

In view of the above remarks, Applicants respectfully submit that claims 1 and 12 are not anticipated by Shaik, and urge that the rejection of claims 1 and 12, and the dependent claims 6 and 7, under 35 U.S.C. § 102(b) be withdrawn.

VI. CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

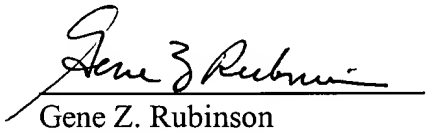
If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: August 29, 2000

By: 

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